COPC

PATENT
Docket No. INTEL/17877

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Ravishankar R. Iyer

U.S. Serial No.: 10/722,884

For: "Methods and Apparatus to Process Cache Allocation Requests Based on Priority"

Filed: November 26, 2003

Assignee: Intel Corporation

Group Art Unit: 2186

Examiner: Matthew A. Bradley

I hereby certify that this paper and the documents referred to as enclosed therewith are being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on this date:

Dated: 12.28.06

Mark G. Hanley
Attorney for Applicant
Registration No. 44,736

TRANSMITTAL OF CERTIFICATE OF CORRECTION

Attn: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Please note the corrections on the enclosed Certificate of Correction. Pursuant to 37 CFR 1.322 (also see MPEP 1480), the applicant respectfully requests issuance of the enclosed Certificate of Correction in view of mistakes in the patent incurred through the fault of the Office.

To evidence the mistakes in the patent incurred through the fault of the Office, the applicant encloses herewith a courtesy copy of the Response to the Office Action Dated January 24, 2006 (the "Response"). In particular, the Response illustrates that the language of issued claim 9 (previously claim 10) recites, in part, "a secondary host application, or a cache allocation request" (see page 5 of the Response).

Additionally, the Response illustrates that the language of issued claim 21 (previously claim 24) recites, in part, "a pre-determined number" (see page 8 of the Response).

Respectfully submitted,

HANLEY, FLIGHT & ZIMMERMAN, LLC
USPTO Customer Number 34431
150 S. Wacker Drive
Suite 2100
Chicago, Illinois 60606
(312) 580-1020

Dated: 12.28.06 By: _____

Mark G. Hanley
Registration No.: 44,736

PTO/SB/44 (04-05)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,103,735

APPLICATION NO.: 10/722,884

ISSUE DATE : September 5, 2006

INVENTOR(S) : Iyer

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 8
Line 2, "and or a cache" should read as --or a cache--.

Column 9
Line 17, "ore-determined" should read as --pre-determined--.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Hanley, Flight & Zimmerman, LLC
150 South Wacker Drive, Suite 2100
Chicago, Illinois 60606

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT
Attorney Docket No.: 20002/17877

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Iyer
U.S. Serial No.	:	10/722,884
Filed	:	November 26, 2003
Title	:	METHODS AND APPARATUS TO PROCESS CACHE ALLOCATION REQUESTS BASED ON PRIORITY
Art Unit	:	2187
Examiner	:	Matthew A. Bradley

I hereby certify that this paper (and/or fee) is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this date:

Dated: **March 24, 2006**

Mark G. Hanley
Registration No. 44,736
Attorney for Applicant

RESPONSE TO THE OFFICE ACTION DATED JANUARY 24, 2006

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Please enter the following amendments and consider the following remarks.

Amendments to the specification begin on page 2 of this paper.

Amendments to the claims are reflected in the listing of the claims that begins on page 3 of this paper.

Remarks begin on page 10 of this paper.

Amendments to the Specification

Please replace paragraph [0002] with the following amended paragraph:

[0002] Typically, cache is memory that a processor may access more quickly than random access memory (RAM) on a main memory chip. Cache may be identified based on how close and accessible a memory is to the processor. For example, a first-level unified (L1) cache may reside on the same chip as the processor. When the processor executes an instruction, for example, the processor first looks at its on-chip cache to find the data associated with that instruction to avoid performing a more time-consuming search for the data elsewhere (e.g., off-chip or on a RAM on a main memory chip).

Listing of the Claims

1. (Currently Amended) A method comprising:

assigning a priority level to a cache allocation request;

identifying an allocation probability associated with the cache allocation request based on the priority level; and

identifying the cache allocation request with one of an allocate condition ~~and~~ or a bypass condition ~~based on the allocation probability~~ by comparing the allocation probability with at least one of a randomly-generated number or a pre-determined number.

2. (Currently Amended) A method as defined in claim 1, wherein assigning the priority level to the cache allocation request comprises assigning the priority level to the cache allocation request based on at least one of stream type, source type, ~~and~~ or a cache occupancy map.

3. (Currently Amended) A method as defined in claim 1, wherein assigning a priority level to the cache allocation request comprises assigning a priority level to at least one of a cache allocation request associated with a primary host application, a cache allocation request associated with a secondary host application, ~~and~~ or a cache allocation request associated with a peripheral application.

4. (Cancelled)

5. (Currently Amended) A method as defined in claim 1, wherein identifying the cache allocation request with one of an allocate condition ~~and~~ or a bypass condition ~~based on the allocation probability~~ comprises identifying the cache allocation request with the allocate condition in response to the allocation probability being greater than ~~or equal to~~ at least one of [[a]] the randomly-generated number ~~and a~~ or the pre-determined number.

6. (Currently Amended) A method as defined in claim 1, wherein identifying the cache allocation request with one of an allocate condition ~~and~~ or a bypass condition ~~based on the allocation probability~~ comprises identifying the cache allocation request with the bypass condition in response to the allocation probability being less than ~~at least one of~~ or equal to at least one of the randomly-generated number ~~and a~~ or the pre-determined number.

7. (Original) A method as defined in claim 1 further comprising allocating a portion of a cache to the cache allocation request in response to identifying the cache allocation request with the allocate condition and denying the cache allocation request in response to identifying the cache allocation request with the bypass condition.

8. (Currently Amended) A machine accessible medium storing instructions, ~~which~~ when executed, cause a processing system to:

assign a priority level to a cache allocation request;

identify an allocation probability associated with the cache allocation request based on the priority level; and

identify the cache allocation request with one of an allocate condition ~~and~~ or a bypass condition ~~based on the allocation probability~~ by comparing the allocation probability with at least one of a randomly-generated number or a pre-determined number.

9. (Currently Amended) A machine accessible medium as defined in claim 8, wherein the instructions, when executed, cause the machine to assign a priority level to the cache allocation request by assigning the priority level to the cache allocation request based on at least one of stream type, source type, ~~and~~ or a cache occupancy map.

10. (Currently Amended) A machine accessible medium as defined in claim 8, wherein the instructions, when executed, cause the machine to assign the priority level to the cache allocation request by assigning a priority level to at least one of a cache allocation request associated with a primary host application, a cache allocation request associated with a secondary host application, ~~and~~ or a cache allocation request associated with a peripheral application.

11. (Cancelled)

12. (Currently Amended) A machine accessible medium as defined in claim 8, wherein the instructions, when executed, cause the machine to identify the cache allocation request with one of the allocate condition ~~and~~ or the bypass condition ~~based on the allocation probability~~ by identifying the cache allocation request with the allocate condition in response to the allocation probability being greater than ~~or equal to~~ at least one of [[a]] the randomly-generated number ~~and a~~ or the pre-determined number.

13. (Currently Amended) A machine accessible medium as defined in claim 8, wherein the instructions, when executed, cause the machine to identify the cache allocation request with one of the allocate condition ~~and~~ or the bypass condition ~~based on the allocation probability~~ by identifying the cache allocation request with the bypass condition in response to the allocation probability being less than or equal to at least one of the randomly-generated number ~~and a~~ or the pre-determined number.

14. (Currently Amended) A machine accessible medium as defined in claim 8, wherein the instructions, ~~which~~ when executed, cause the machine to allocate a portion of a cache to the cache allocation request in response to identifying the cache allocation request with the allocate condition, and to deny the cache allocation request in response to identifying the cache allocation request with the bypass condition.

15. (Currently Amended) A machine accessible medium as defined in claim 8, wherein the machine readable medium comprises one of a programmable gate array, application specific integrated circuit, erasable programmable read only memory, read only memory, random access memory, magnetic media, ~~and~~ or optical media.

16. (Currently Amended) An apparatus comprising:

a cache to store one or more data blocks of cache allocation requests;

a priority assignment unit to assign a priority level to a cache allocation request; and

a cache controller to identify an allocation probability associated with the cache allocation request based on the priority level, and to identify the cache allocation request with

one of an allocate condition ~~and~~ or a bypass condition ~~based on the allocation probability~~ by comparing the allocation probability with at least one of a randomly-generated number or a pre-determined number.

17. (Currently Amended) An apparatus as defined in claim 16, wherein the cache allocation request comprises at least one of a cache allocation request associated with a primary host application, a cache allocation request associated with a secondary host application, ~~and~~ or a cache allocation request associated with a peripheral application.

18. (Currently Amended) An apparatus as defined in claim 16, wherein the priority assignment unit comprises at least one of an operating system, a compiler, ~~and~~ or an application specific integrated circuit.

19. (Currently Amended) An apparatus as defined in claim 16, wherein the cache controller is to assign the priority level to the cache allocation request based on at least one of stream type, source type, ~~and~~ or a cache occupancy map.

20. (Cancelled)

21. (Currently Amended) An apparatus as defined in claim 16, wherein the cache controller is to identify the cache allocation request with the allocate condition in response to the allocation probability being greater than ~~or equal to~~ at least one of [[a]] the randomly-generated number ~~and a~~ or the pre-determined number.

22. (Currently Amended) An apparatus as defined in claim 16, wherein the cache controller is to identify the cache allocation request with the bypass condition in response to the allocation probability being less than ~~at least one of~~ or equal to at least one of the randomly-generated number ~~and a~~ or the pre-determined number.

23. (Original) An apparatus as defined in claim 16, wherein the cache controller is to allocate a portion of the cache to the cache allocation request in response to identifying the cache allocation request with the allocate condition.

24. (Currently Amended) A processor system comprising:

a static random access memory (SRAM) to store one or more data blocks of cache allocation requests; and

a processor coupled to the SRAM, the processor to:

assign a priority level to a cache allocation request;

identify an allocation probability associated with the cache allocation request based on the priority level; and

identify the cache allocation request with one of an allocate condition and a bypass condition ~~based on the allocation probability~~ by comparing the allocation probability with at least one of a randomly-generated number or a pre-determined number.

25. (Currently Amended) A processor system as defined in claim 24, wherein the cache allocation request comprises at least one of a cache allocation request associated with a primary host application, a cache allocation request associated with a secondary host application, ~~and~~ or a cache allocation request associated with a peripheral application.

26. (Currently Amended) A processor system as defined in claim 24, wherein the processor is to assign the priority level to the cache allocation request based on at least one of stream type, source type, ~~and~~ or a cache occupancy map.

27. (Cancelled)

28. (Currently Amended) A processor system as defined in claim 24, wherein the processor is to identify the cache allocation request with the allocate condition in response to ~~in response to~~ the allocation probability being greater than ~~or equal to~~ at least one of [[a]] the randomly-generated number ~~and a~~ or the pre-determined number.

29. (Currently Amended) A processor system as defined in claim 24, wherein the processor is to identify the cache allocation request with the bypass condition in response to the allocation probability being less than or equal to at least one of the randomly-generated number ~~and a~~ or the pre-determined number.

30. (Original) A processor system as defined in claim 24, wherein the processor is to allocate a portion of the SRAM to the cache allocation request in response to identifying the cache allocation request with the allocate condition.

REMARKS

The applicant has carefully considered the official action dated January 24, 2006, and the references it cites. In the official action, the specification was objected to, claims 1-30 were objected to, claims 1-3, 7, 16-19, 23-26, and 30 were rejected under 35 U.S.C. 102(a) and 35 U.S.C. 102(e) as anticipated by Harris (U.S. Patent No. 6,601,151), claims 8-10, 14, and 15 were rejected under 35 U.S.C. 103(a) as unpatentable over Rubinstein (U.S. Patent No. 5,913,215) in view of Harris, and claims 4-6, 11-13, 20-22, and 27-29 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

By way of this response, paragraph [0002] of the specification has been amended to correct two minor omissions, claims 5, 12, 21, and 28 have been amended to remove the language "or equal to," claims 6, 13, 22, and 29 have been amended to include the language "or equal to" that was previously and erroneously included in claims 5, 12, 21, and 28, claim 28 has been amended to correct a minor typographical error, claims 4, 11, 20, and 27 have been cancelled without prejudice, and additional amendments have been made to claims 1-3, 6, 8-10, 13-19, 22, 24-26, and 29. In view of the foregoing amendments and the following remarks, the applicant respectfully traverses the outstanding rejections and respectfully submits that all pending claims are in condition for allowance. Favorable reconsideration is respectfully requested.

Turning to the objections to claims 1-30, as described by the official action (pages 2-3), the applicant wishes to correct statements made by the examiner on the top of page 3 of the official action. In particular, language of the official action reads, "As per the specification...if the randomly-generated number is greater than the allocation probability

number, then the allocation takes place." [Official action, page 3, lines 2-5]. This statement is incorrect. On the contrary, as correctly noted by the examiner in the Official action, "if the AP is greater than the random number, then the cache controller allows allocation...if the AP is less than or equal to the random number, the cache controller denies the allocation..." [Official action, page 3, lines 13-16]. Accordingly, the applicant has amended dependent claims 5, 12, 21, and 28 to remove the language "or equal to," which is, instead, now added to dependent claims 6, 13, 22, and 29.

Turning to the art rejections, the applicant respectfully submits that independent claim 1, as amended, is allowable over the art of record. As amended, independent claim 1 is now directed to a method comprising, *inter alia*, identifying the cache allocation request with one of an allocate condition or a bypass condition by comparing the allocation probability with at least one of a randomly-generated number or a pre-determined number. None of the cited references teaches or suggests identifying the cache allocation request with one of an allocate condition or a bypass condition by comparing the allocation probability with at least one of a randomly-generated number or a pre-determined number. In particular, independent claim 1 now incorporates subject matter indicated as allowable in the official action.

Accordingly, the applicant submits that claim 1, and claims 2, 3, and 5-7 dependent thereon, are now in condition for allowance.

Independent claim 16, as amended, is also allowable over the art of record for reasons similar to those set forth above in connection with independent claim 1. Specifically, claim 16 recites, *inter alia*, an apparatus comprising a cache controller to identify the cache allocation request with one of an allocate condition or a bypass condition by comparing the allocation probability with at least one of a randomly-generated number or a pre-determined

number. The applicant submits that the rejection of claim 16, and claims 17-19, and 21-23 dependent thereon, must be withdrawn for at least the reasons set forth above in connection with claim 1.

Independent claim 24, as amended, is also allowable over the art of record for reasons similar to those set forth above in connection with independent claims 1 and 16. Specifically, claim 24 recites, *inter alia*, a processor system comprising a processor coupled to the SRAM, the processor to identify the cache allocation request with one of an allocate condition and a bypass condition by comparing the allocation probability with at least one of a randomly-generated number or a pre-determined number. The applicant submits that the rejection of claim 24, and claims 25, 26, and 28-30 dependent thereon, must be withdrawn for at least the reasons set forth above in connection with claims 1 and 16.

The applicant respectfully submits that independent claim 8, as amended, is allowable over the art of record. As amended, independent claim 8 is now directed to a machine accessible medium storing instructions, when executed, cause a processing system to, *inter alia*, identify the cache allocation request with one of an allocate condition or a bypass condition by comparing the allocation probability with at least one of a randomly-generated number or a pre-determined number. None of the cited references teaches or suggests identifying the cache allocation request with one of an allocate condition or a bypass condition by comparing the allocation probability with at least one of a randomly-generated number or a pre-determined number. In particular, independent claim 8 now incorporates subject matter indicated as allowable in the official action.

Accordingly, claim 8, and claims 9, 10, and 12-15 dependent thereon, are now in condition for allowance.

In view of the foregoing, the applicant respectfully submits that this application is now in condition for allowance. If there are any remaining matters that the examiner would like to discuss, the examiner is invited to contact the undersigned representative at the telephone number set forth below.

Respectfully submitted,

Mark G. Hanley
Registration No. 44,736
Hanley, Flight & Zimmerman, LLC
(at customer number 34431)
20 North Wacker Drive
Suite 4220
Chicago, Illinois 60606
312.580.1020

Dated: **March 24, 2006**